Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 8. (Canceled).

9. (Previously Presented) A semiconductor system comprising:

a pn transition; and

a chip having an edge region, the chip including a first layer of a first conductivity type and a second layer of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region and a center region, the pn transition being provided between the first layer and the second layer;

wherein the second layer is more weakly doped in the edge region than in the center region, and the boundary surface of the pn transition is non-parallel to the main chip plane at the edge region.

10. (Currently Amended) The semiconductor system of claim [[9]] 11, wherein the pn transition includes a diode.

11. (Currently Amended) [[The]] A semiconductor system ~~of claim 9,~~ comprising:

a pn transition; and

a chip having an edge region, the chip including a first layer of a first conductivity type and a second layer of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region and a center region, the pn transition being provided between the first layer and the second layer;

wherein the second layer is more weakly doped in the edge region than in the center region, and the boundary surface of the pn transition is non-parallel to the main chip plane at the edge region; and

wherein the boundary surface of the pn transition includes a positive beveling angle at the edge region.

12. (Currently Amended) The semiconductor system of claim [[9]] 11, wherein the boundary surface of the pn transition is curved at the edge region.

13. (Currently Amended) The semiconductor system of claim [[9]] 11, wherein a thickness of the chip is less at the edge region than in the center region.

14. (Previously Presented) A method for manufacturing a semiconductor system, comprising:

forming a pn transition;

forming a chip having an edge region, the chip including a first layer of a first conductivity type and a second layer of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region and a center region, the pn transition being provided between the first layer and the second layer; and

doping the second layer more weakly in the edge region than in the center region, wherein a boundary surface of the pn transition is non-parallel to the main chip plane at the edge region; and

wherein the first layer is manufactured using patterned doping.

15. (Previously Presented) The method of claim 14, wherein the patterned doping is provided by pre-coating the chip with dopant, subsequently removing the coating in a sub-region of the chip, and subsequently introducing the dopant into the chip.

16. (Currently Amended) The method of claim [[14]] 15, wherein the coating is removed by sawing.

17. (Previously Presented) The method of claim 16, wherein the sawing is performed with at least one of a diamond saw and water-supported laser cutting.

18. (Previously Presented) The method of claim 14, wherein the chip is pre-coated with dopant via at least one of APCVD deposition of a doped glass, a doping film, a gas phase coating, ion implantation, and an application of doping pastes.